REMARKS

Reconsideration and allowance of the present patent application based on the following remarks are respectfully requested.

By this Amendment, the specification and claims 2-13 and 15-23 are amended. Support for the amendments can be found throughout the original disclosure. No new matter has been added. Accordingly, after entry of this Amendment, claims 1-23 will remain pending in the patent application.

In the Office Action, the disclosure was objected to. In response, the specification has been amended to add the section headings "FIELD", "BACKGROUND", "SUMMARY", "BRIEF DESCRIPTION OF THE DRAWINGS" and "DETAILED DESCRIPTION". This amendment to the specification obviates the objection. Accordingly, reconsideration and withdrawal of the objection to the disclosure are respectfully requested.

In the Office Action, claims 2-13 and 15-23 were objected to. In response, claims 2-13, 15-19 and 21-23 have been amended in the manner suggested by the Office. Accordingly, reconsideration and withdrawal of the objection to claims 2-13 and 15-23 are respectfully requested.

Claim 15 was rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement. The rejection is respectfully traversed.

In connection with the rejection, the Office asserts that claim 15 is a single means claim and that the claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully disagrees.

First, claim 15 is *not* a single means claim because claim 15 is in combination with another recited element. Indeed, claim 15 depends from claim 14 and thus contains all of the recitations set forth in claim 14. For example, claim 15 recites a data writing means for writing the at least two replica editions, which replica editions have been generated by the data replication means recited in claim 14. Thus, claim 15 is in combination with another recited element and, therefore, is *not* a single means claim.

Second, the specification teaches those skilled in the art how to make and use the full scope of the claimed invention *without undue experimentation*. *See* MPEP 2164.01. As a non-limiting example, one embodiment described at page 16, lines 3-14 of the present application discloses a channel merge function 68 that is provided to receive the output from multiplexers 64_0 to 64_3, merge the data on four internal channels into a merged serial data

stream and then provide the merged serial data stream to a host for writing to the memory of the host. Thus, a clear example is given as to what is encompassed by the data replication means (multiplexers 62_0 to 62_3 – *see* present application at page 15, lines 1-4) and the data writing means (channel merge function 68). In addition, as stated at page 15, lines 20-27 of the present application, in a preferred example, the replication units are embodied in hardware such as an FPGA. Thus, the subject matter recited is described in such a way as to enable one skilled in the art to make and/or use the invention *without undue experimentation*. Clearly, the as-filed disclosure contains sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention.

Accordingly, reconsideration and withdrawal of the rejection of claim 15 under 35 U.S.C. §112, first paragraph, are respectfully requested.

Claims 20-23 were rejected under 35 U.S.C. §112, second paragraph. In response to this rejection, claim 20 has been rewritten in independent form to include the features of claim 14. The amendment to claim 14 obviates the rejection. Claims 21-23 are patentable at least by virtue of their dependency from claim 20.

Accordingly, reconsideration and withdrawal of the rejection of claims 20-23 under 35 U.S.C. §112, second paragraph, are respectfully requested.

Claims 1-20 were rejected under 35 U.S.C. §102(a), based on the SCAMPI Prototype Implementation Report D2.2 published on November 16, 2003 (hereinafter D22). The rejection is respectfully traversed.

Claim 1 recites a method of processing data, the method comprising, *inter alia*, "replicating said data on board a network analyser card to produce at least two editions of the received data; and writing said editions of the received data to an area of memory in a host that is directly accessible by a host application."

These aspects of claim 1 are amply supported by the original disclosure. As a non-limiting example, one embodiment of the invention discloses that data received by the network analyser card 32 from the network is replicated by the network analyser card 32 and provided to the memory 38. *See* present application at page 11, lines 33-34, page 12, lines 1-15 and Figure 2. The originally received data is replicated such that N editions of the data are generated and all are written to the memory 38 in such a way that the processors 34_1 to 34_N between them running the IDS application can access the data directly. This means that in contrast to conventional systems in which data is received into kernel space of a memory and then copied by the operating system into application space for use by associated processors,

in the present case the data may be accessed directly from the physical location to which it was written by the network analyser card 32. Accordingly, host processing capacity is *not* required for copying data from the physical kernel space to the physical application space of the host memory. *Id.* As a result, the host processor or processors can assign a greater proportion of their processing capacity to applications running on the host. *See* present application at page 5, lines 30-33 and page 6, lines 1-6.

With this said, there is nothing in the cited portions of D22 that remotely discloses, teaches or suggests these aspects of claim 1. In order to establish a *prima facie* rejection , "the identical invention must be shown in as complete detail as is contained in the ... claim." *See* MPEP § 2131, citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), emphasis added. MPEP § 2131 also indicates that "the elements must be arranged as required by the claim." *See* MPEP § 2131, citing In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990), emphasis added. Further, "unless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102." Net MoneyIN, Inc. *v. VeriSign*, Inc. et al., Slip Op. pg. 17-18 (Fed. Cir., October 20, 2008), emphasis added. The Office Action does not meet these requirements.

The Office refers to page 55 of D22 as allegedly disclosing, teaching or suggesting the step of replicating data on board a network analyzer card. *See* Office Action at page 4. The Office further refers to pages 18 and 19 of D22 as allegedly disclosing, teaching or suggesting the production of at least two editions of the data. *See* Office Action at page 5. The Office also refers to pages 19 and 25 and section 2.7.4 of D22 as allegedly disclosing, teaching or suggesting the step of "writing said editions of the received data to an area of memory in a host that is directly accessible by a host application." Applicant respectfully disagrees.

Referring first to page 55 of D22, those cited portions merely disclose a conventional interface card, referred to as the "COMBO6". The COMBO6 is said to include an FPGA chip, various memory modules, a PCI bus interface, a daughterboard interface and auxiliary circuits. However, there is *no* disclosure whatsoever of anything arranged to *replicate received data and produce two editions of the data*, as recited in claim 1.

Referring now to pages 18 and 19 and in particular Figure 2.6, those cited portions state that:

> *"For all applications willing to receive a packet flow, a unique packet buffer is assigned. These packet buffers are implemented in shared memory between the Click modular router and the application. All required packets are copied to the appropriate buffers by the Click element to buffer()."*

On page 19 it is stated that:

> *"the buffer is implemented using a circular buffer in shared memory. The Click element toBuffer copies... packets to this buffer and the MAPI function get_next_packet () reads elements out of it...".*

With this said, nowhere do those cited portions of D22 disclose, teach or suggest replicating data packets on board a network analyzer card, as recited in claim 1. In fact, Applicant wishes to point out that the description of the Click modular router with reference to Figure 2.6 is within the overall section in the document entitled "2.6 Middleware". This section begins on page 16 of D22. The "middleware" of Figure 2.6 is represented in the "Generic Architectural Decomposition" of the SCAMPI architecture as defined in "deliverable D1.2". *See* D22 at Figure 2.1 and page 7.

Now, referring to Figure 2.1 in D22, the "monitoring hardware", "network processor" and "intelligent routers" are all shown as *separate and distinct from the middleware*. There is *no* teaching whatsoever of the provision of data replication on the network analyzer card itself. Indeed, as discussed in section 2.2 on page 7 of D22, it appears that the "SCAMPI adaptor" or "DAG cards", which might be referred to as the network analyzer cards (although Applicant disagrees) and are given as examples of the hardware shown in Figure 2.1, are *separate* from the middleware where the "data copying", to which the Office refers, takes place. Thus, D22 does *not* disclose the step of replicating the data on board a network analyzer card.

Furthermore, there is *no* disclosure whatsoever in the description on pages 18 and 19 of D22 of making at least two editions of received data and writing this to an area of memory in a host that is directly accessible by host application. In particular, there is no disclosure of producing "*at least two editions*", as recited in claim 1. The description on page 18 merely states that "*required packets are copied to the appropriate buffers by the click element toBuffer*". This description of D22 does *not* disclose, teach or suggest that *plural copies of any single data packet* are made and copied to more than one of the buffers. It merely says that the data, which is a packet that has been filtered, is then copied to a buffer associated with a particular application.

Applicant respectfully submits that page 19, paragraph 1, line 1, refers to the fact that "***the*** buffer is implemented using a circular buffer in shared memory". To understand quite how this operates, the Office's attention is directed at the next SCAMPI document in the sequence, "SCAMPI Deliverable D2.3" (cited by Applicant in the IDS filed on April 21, 2006, hereinafter "D23") and page 45 thereof where it is stated "***To avoid the cost of copying a packet*** *received by a regular NIC multiple times (once for each flow that monitors the interface) we have introduced a common buffer where packets are being stored and is shared between the applications monitoring the same interface,*" emphasis added. Thus, the SCAMPI methodology clearly *teaches away* from copying packets by the network interface cards and instead employs a "circular buffer" in which packets are stored and to which applications have access. The SCAMPI methodology, as disclosed in D22 and further explained in D23, does *not* involve multiple copying of data packets to separate buffers but merely the "copying" to, or writing to, an application specific area of memory on a host, a specific data packet. Notably, this is not a disclosure of the generation of at least two editions of the same data and then the writing of the two editions to host memory. There is *no* disclosure in D22 of the above identified aspects of claim 1. Applicant respectfully submits that D22 is similar to the prior art discussed at page 5, lines 22-28 of the present application where it is stated that "[in] conventional systems in which data is written to a host memory and then copied from one part of the host memory to another for processing."

Accordingly, for at least these reasons, claim 1 is patentable over the cited portions of D22.

Claims 2-13 are patentable over the cited portions of D22 at least by virtue of their dependency from claim 1 and for the additional features recited therein.

Claim 14 is patentable over the cited portions of D22 for at least similar reasons as provided above for claim 1 and for the features recited therein. For example, the cited portions of D22 do not disclose, teach or suggest a network analyser card for connection to a host and a network, the card comprising, *inter alia*, "...data replication means for generating at least two replica editions of the received data frames..."

Claims 15-19 are patentable over the cited portions of D22 at least by virtue of their dependency from claim 14 and for the additional features recited therein.

Claim 20 is patentable over the cited portions of D22 for at least similar reasons as provided above for claim 1 and for the features recited therein. For example, the cited portions of D22 do not disclose, teach or suggest a host for connection to a network, the host

comprising, *inter alia*, "at least two processors for processing said editions of the received data, wherein the network analyser card includes ...data replication means for generating at least two replica editions of the received data frames..."

Accordingly, reconsideration and withdrawal of the rejection of claims 1-20 under 35 U.S.C. §102(a) based on D22 are respectfully requested.

Claims 21-23 were rejected under 35 U.S.C. §103(a) based on D22 in view of U.S. Pat. No. 4,837,735 to Allen *et al.* (hereinafter Allen). The rejection is respectfully traversed.

Claims 21-23 are patentable over the cited portions of D22 at least by virtue of their dependency from claim 20 and for the additional features recited therein.

The cited portions of Allen fail to cure the deficiencies of D22. The cited portions of Allen relate to a parallel processing system. The cited portions of Allen do not disclose, teach or suggest the aspect of data replication on board a network analyzer card, as recited in claims 20-23. Thus, any proper combination of D22 and Allen cannot result, in any way, in the inventions of claims 20-23.

Along these lines, Applicant respectfully submits that Allen is related to a general processor arrangement and is in a different technical area from D22 that relates to network monitoring. Thus, in the absence of hindsight based on Applicant's own disclosure, there is no motivation or suggestion for one skilled in the art to combine the teachings of D22 and Allen. Therefore, for at least this additional reason, claims 20-23 are not obvious in view of D22 and Allen.

Accordingly, reconsideration and withdrawal of the rejection of claims 21-23 under 35 U.S.C. §103(a) based on D22 in view of Allen are respectfully requested.

Applicant has addressed the Examiner's rejections and objection and respectfully submits that the application is in condition for allowance. A notice to that effect is earnestly solicited.

If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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